AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor test apparatus comprising:

an input data generating unit that generates ~~first~~ measurement data to be applied to a test semiconductor device for testing functions of the test semiconductor device based on first input measurement conditions;

an expected data generating unit that generates expected data for ~~said input data under input first~~ the measurement data ~~conditions~~ based on the first input measurement condition;

a determination unit that compares measurement result data obtained from the test semiconductor device based on the measurement data with the expected data ~~based on said measurement data~~ and determines whether the ~~function of said~~ test semiconductor device is a pass or failure, and outputs the data of the determination result ~~data~~ as ~~a~~ determination result data; and

a data log system ~~unit~~ that writes into a log memory in a time sequence ~~first~~ associated data for a test semiconductor device that includes said determination result data, ~~first measurement result data,~~ said measurement ~~expectation~~ expected data, and said measurement ~~input~~ data;

wherein said input data generating unit presets said log system with a write termination condition for terminating writing into the data log memory when the test result of a test semiconductor device is a failure or when all test results of the function test of a test semiconductor device have been completed, and said input data generating unit also presets a write extension condition for extending the writing into the data log memory when the test result of a test semiconductor device becomes a failure before all function tests for the test semiconductor device have been completed or when the address of the data log memory has not been completed,

wherein said data log system ~~unit writes a second associated data that includes second measurement result data for a semiconductor test device that is determined as a failure into the log memory for a predetermined period even after any of said first~~

~~associated data or the address of the log memory satisfy preset write termination conditions that terminate the writing~~ continues the writing of subsequent associated data of the test semiconductor device into the log memory over an extended period of time according to the write extension condition until said write termination condition is satisfied.

2. (Currently amended) ~~A~~ The semiconductor test apparatus according to claim 1 wherein said data log system continues to write ~~said second~~ associated data ~~including a second measurement data~~ into the data log memory over an extended time range indicated by ~~input~~ the write extension conditions even after the write termination conditions have been satisfied~~,~~

~~wherein the second measurement data includes results of measurement for analysis of the failure~~.

3. (Currently amended) ~~A~~ The semiconductor test apparatus according to claim 1 wherein said data log system writes said ~~first~~ associated data into a predetermined address of the log memory at each time unit in which ~~the~~ it is determined whether a test semiconductor device is ~~a~~ pass or ~~a~~ failure.

4. (Currently amended) ~~A~~ The semiconductor test apparatus according to claim 1 wherein said log memory has a predetermined address range, and is structured so as to overwrite ~~the second~~ subsequent associated data for a subsequent semiconductor device from the head address after writing the associated data ~~in~~ of a test semiconductor device into the final address.

5. (Currently amended) ~~A~~ The semiconductor test apparatus according to claim 1 wherein said data log system increments the address of said log memory at each time unit in which it is determined whether the test semiconductor device being tested is ~~a~~ pass or ~~a~~ failure, and writes in sequence said associated data.

6. Cancelled.